Cache Memory

address a, r 3 ports

1) direct mapped cache (E = 1)
2) associative cache \( (s=1) \)

Diagram:

- Top: Key, Block
- Bottom: Address

Tags and Block Offset
3) set associative

\[
\begin{array}{c}
\text{key} \\
\downarrow \\
S
\end{array}
\]

\[
\begin{array}{c}
\text{block}
\end{array}
\]

(\(S > 1 \text{ and } k \leq S\))

\[
\begin{array}{c}
\text{key} \\
\downarrow \\
\text{block}
\end{array}
\]

\[
\begin{array}{c}
\text{block}
\end{array}
\]

Total size is \(S \times E \times 3\) bytes

If \(E = 2\), called

2-way set associative
AMP Opteron

64KB L1 cache icache 2-way assoc. 64KB
64KB L1 cache d-cache
1MB L2 cache unified 16-way

per block