Instruction Set Architecture (ISA) - programmer's view of the processor
- Instruction Set
- Register file
- Memory
- Operating modes

x86 ISA

Instructions
- arithmetic
- control flow
- Boolean ops
- shift
- compare
- memory

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0256

Register file (4 classes of registers in x86)
- data/general reg.
- address/index reg.
- segment reg.
- status reg.
Data/generic named A (accumulator), B (base), C (counter), and D (data).

Addr. reg. named DI (destination index), SI (source index), SP (stack pointer), and BP (base pointer).

Names SP + BP are relevant!

Segment registers
- CS  code segment
- DS  data segment
- SS  stack segment
- ES, FS, GS  extra segments
Status registers
- IP: instruction pointer
- FLAGS: flags register
- ZERO
- SIGN
- CARRY
- OVERFLOW
- INTERRUPT

Memory organization
- Memory is byte addressable
- Multi-byte elements, the address is lowest addr, the element occupies
  e.g., 32-bit word in 0x500, 0x501, 0x502, 0x503
  addr. of word is 0x500

Little endian vs. big endian
- Little endian - least significant byte (LSB) goes in lowest address
  "Little end first"
- Big endian - most significant byte (MSB) goes in lowest address
  "Biggest end first"

<table>
<thead>
<tr>
<th>Little</th>
<th>Big</th>
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</thead>
<tbody>
<tr>
<td>LSB 4-byte</td>
<td>m15</td>
</tr>
<tr>
<td>m8 6-byte</td>
<td>m15</td>
</tr>
<tr>
<td>m8</td>
<td>m31</td>
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