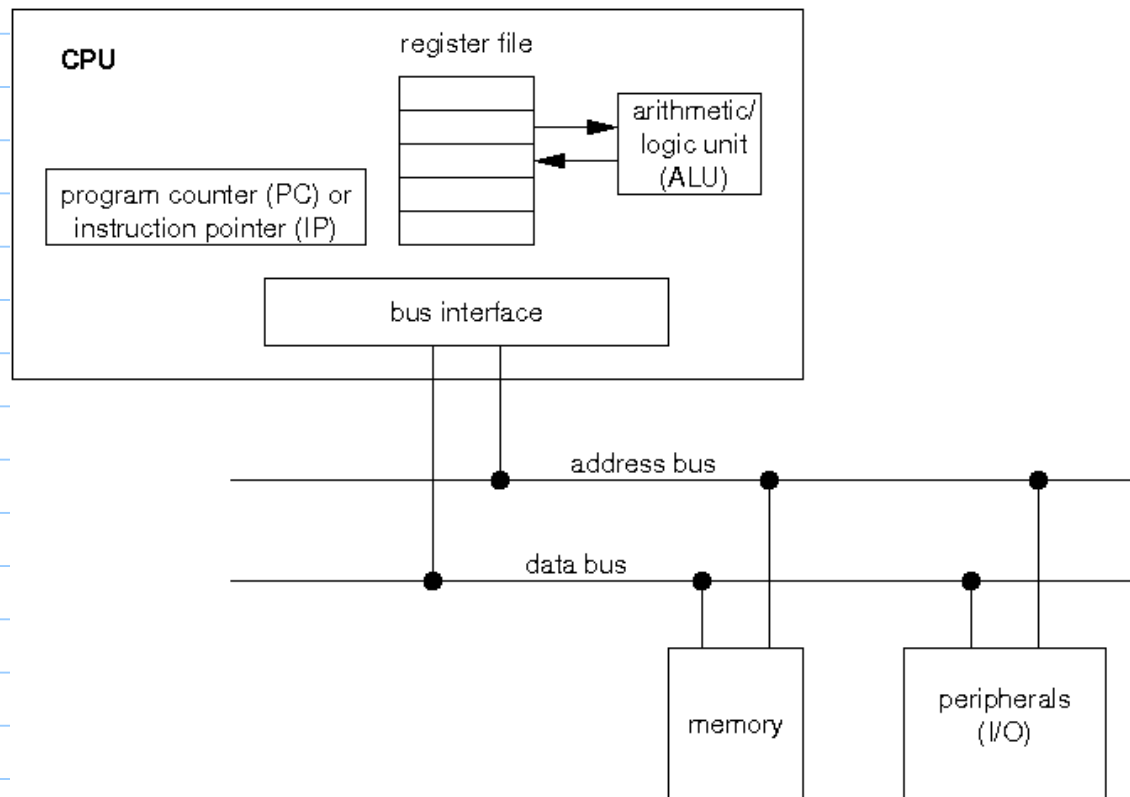


# Hardware and Instruction Set Architecture

Note Title

9/9/2008



fetch  
decode  
execute

# Instruction Set Architecture (ISA)

programmer's view of the processor

- Instruction Set
- Register file
- Memory
- Operating modes

x86 ISA

8086

Instructions

80186

80286

- arithmetic

- control flow 80386

- Boolean ops

- peripheral access

- shift

- conversion Pentium

- compare

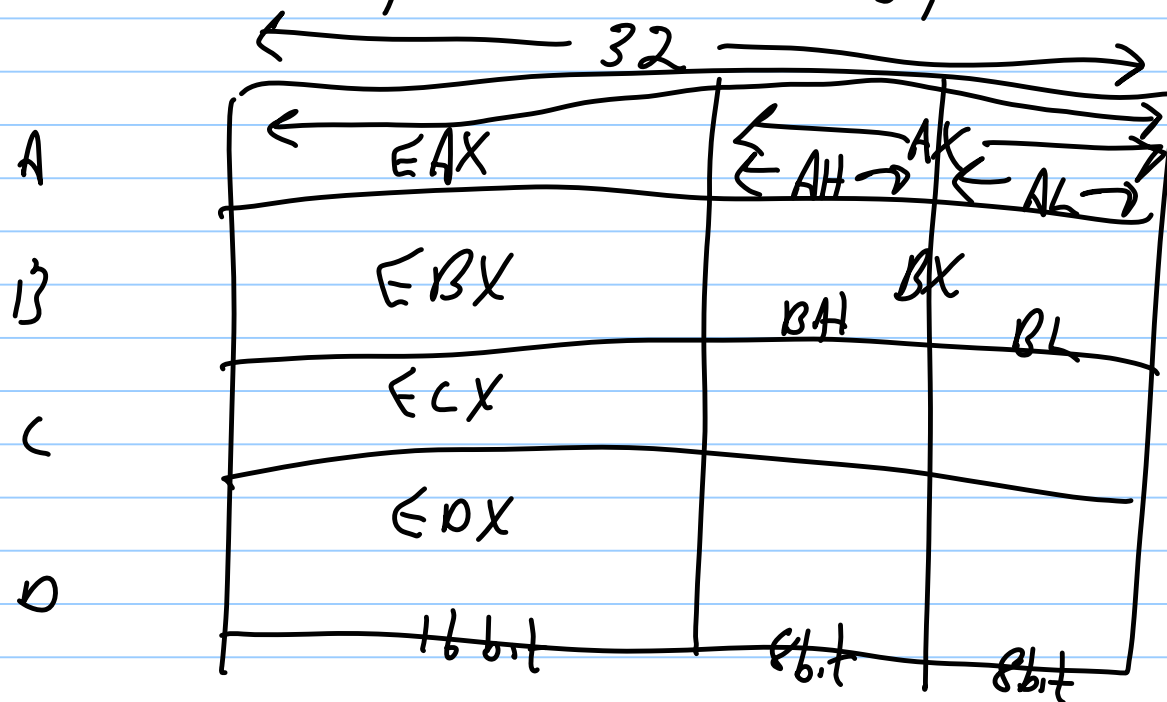
- system

- memory

register file (4 classes of register in x86)

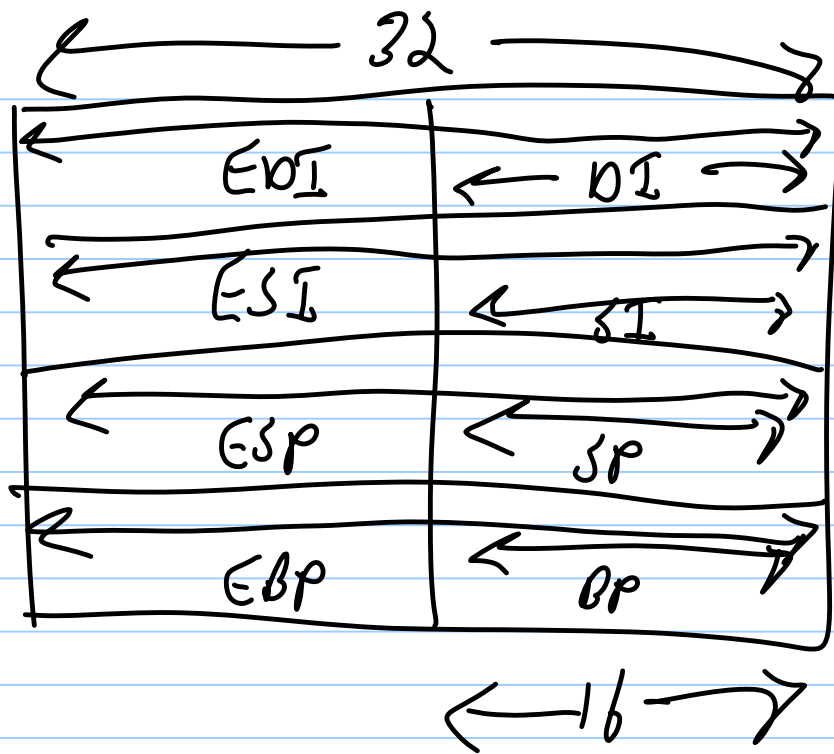
- data/general reg.
- address/index reg.
- segment reg.
- status reg.

Data/general named A (accumulator),  
B (base), C (counter), and D (data).



addr. reg. named DI (destination index),  
SI (source index), SP (stack pointer), and  
BP (base pointer)

Names SP & BP are relevant!



## Segment registers

CS code segment

DS data segment

SS stack segment

ES, FS, GS extra segments

## Status registers

IP instruction pointer

FLAGS flags register

ZERO

SIGN

CARRY

OVERFLOW

INTERRUPT

## Memory organization

memory is byte addressable

multi-byte elements, the address is lowest addr. the element occupies

e.g., 32-bit word in  $0x500, 0x501, 0x502, 0x503$   
addr. of word is  $0x500$

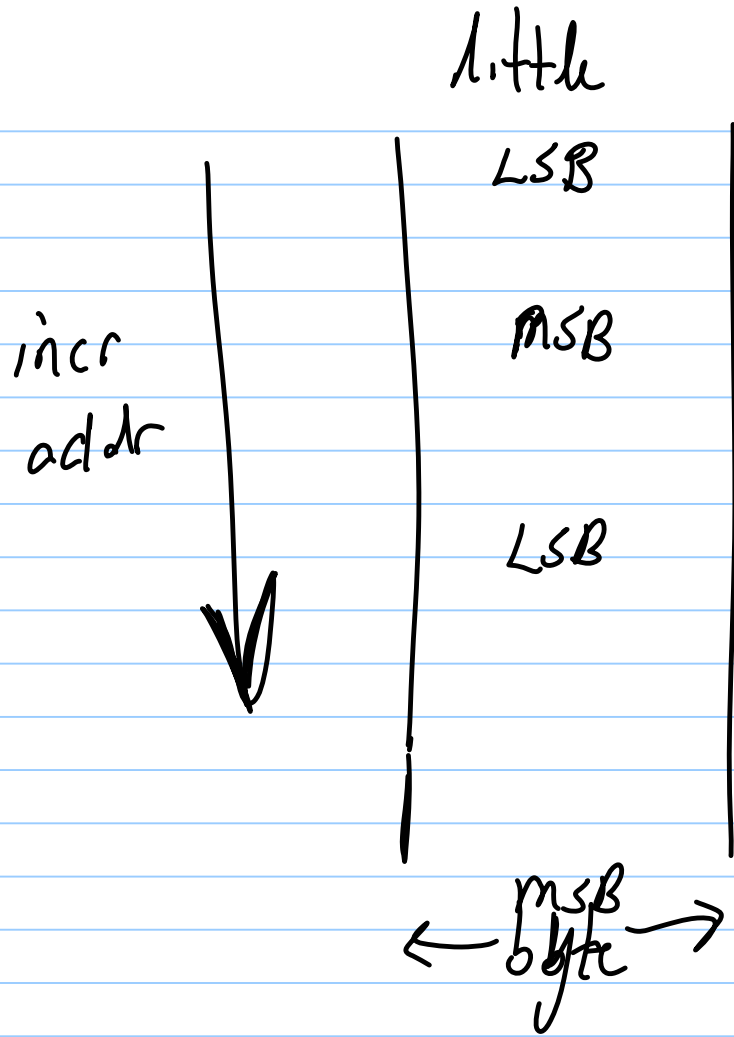
little endian vs. big endian

little endian - least significant byte (LSB)  
goes in lowest address

"littlest end first"

x86 big endian most significant byte (MSB)  
goes in lowest address

"biggest end first"



4 byte  
element

8 byte  
element

