Simbench: A Logic Simulation Benchmark Set

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1. Introduction

The academic research community has been investigating the parallel execution of discrete-event simulation models in general [1] and logic simulation models in particular [2] for more than a decade. Yet, in spite of these efforts, production logic simulators today are almost exclusively executed on uniprocessor systems. The lack of adoption of parallel implementations by the commercial community has a number of causes:

- Historically, parallel computer systems were expensive to acquire and difficult to maintain. This impediment to adoption has clearly been diminished in recent years, with the availability of relatively inexpensive symmetric multiprocessor systems from a number of manufacturers.
- The research community has not used industry standard languages (e.g., VHDL and/or Verilog) in its experimental parallel simulator implementations. A clear exception to the above is the work of Wilsey et al. at the University of Cincinnati, which uses VHDL [3].
- There is a lack of an appropriate set of example simulations that can be used to effectively test both the usefulness of new algorithmic ideas and the performance of experimental implementations.

It is this last issue that we wish to address here. We are proposing the collection of a benchmark set of simulation applications, specified in VHDL, which is freely distributable to the research community. These simulation applications should be realistic digital system design examples that exercise the simulation system in a manner that is common to current design practice.

In this paper, we describe the current practice of the simulation research community, discuss the desirable properties to be present in a new benchmark set, and describe our efforts toward the development of this new benchmark set. We call the new benchmark SIMBENCH.

2. Background

The current practice in the parallel simulation research community for experimentation with logic simulation systems is the use of the ISCAS benchmark set, synthetic benchmarks, or locally available circuits. The ISCAS benchmarks (both the combinational set [4] and the sequential set [5]) were originally developed as benchmarks for place-and-route algorithms, not simulation systems. As a result they include topology descriptions, but the functionality of the circuits is not disclosed. Without the availability of realistic input test vectors, the simulation community has resorted to the use of random input vectors, with a unit delay timing model. In addition, the size of the circuits is relatively small (up to 18,000 components). All of the above

facts tend to compromise the usefulness of the ISCAS benchmark circuits for investigating parallel logic simulation.

The second common practice is the use of synthetic benchmark circuits. Either randomly generated circuit graphs or regular arrays of circuit primitives are automatically synthesized as test circuits. Here, the size of the circuit can easily be scaled up to arbitrary levels; however, neither the circuit topologies or the input test vector sets are particularly indicative of the types of simulations that real designers execute when developing real systems.

In an attempt to address the issue of realism in the tests, many researchers have exploited individual circuits that are locally available at their home institution. Here, the credibility of the circuit as a reasonable exercise of the simulator is improved, but these locally available circuits are often small, and (most importantly) they are not typically available to the entire research community. This last issue is crucial, since independent researchers must corroborate the conclusions that are reached in any experimental research before those conclusions can be completely relied upon. The conclusions reached by two distinct research groups might be different simply because they are not using the same inputs into the experiment.

In spite of the obvious limitations in the above, this represents the current practice of the academic research community investigating parallel logic simulation. As a service to this research community, and in an attempt to make its investigations more relevant to real commercial practice, we believe that a new set of benchmark circuits should be gathered, maintained, and freely disseminated for research use.

3. Features of a New Simulation Benchmark

A new benchmark set, to be maximally useful, must address all of the limitations alluded to in the above section. Specifically, we need to have the following features present:

- The benchmark set must be freely distributable to the entire research community. This is crucial to the reproducibility of research results.
- A significant fraction of the circuits in the benchmark set must be of sufficient size as to make parallel execution of their simulation models desirable to the user community. Simulations that complete in less than one minute are not the target systems. We are interested in improving the execution time associated with simulations that run for multiple hours.
- The benchmark set must not only include topology information for a circuit, but also input vectors that exercise the circuit.
- The benchmark simulations must represent a realistic match with current (and future) practice in the way that actual users take advantage of simulation tools.
- The circuits must come from a variety of sources, and represent a variety of designers and design styles.

Free distribution of the benchmark set is definitely an essential element in its overall usefulness. This comes in two parts. First, the original contributors of the circuits must allow them to be disseminated without undue restriction (e.g., a restriction that their use be limited to research

purposes would be considered reasonable). Second, the cost to individual research groups should be held to an absolute minimum. We plan to make the benchmark set available via the web at no cost to users (i.e., see http://ccrc.wustl.edu/~simbench).

The benefit to the user community of faster simulation execution is only an issue for those simulations that currently take a significant amount of time to execute. For this reason, the bulk of the circuits in the benchmark set should be fairly significant in size. Alternatively, relatively small circuits that have the need to simulate a long input vector set are also candidates for inclusion in the benchmark.

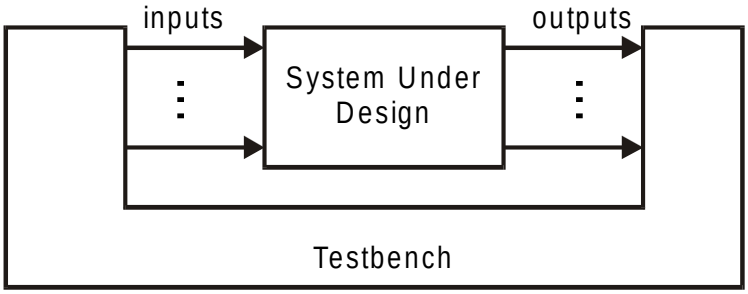

Figure 1. Providing input test vectors.

The need to incorporate input test vectors with the circuits can be most easily addressed through the use of a testbench included in the VHDL code for distribution. Figure 1 illustrates the use of a testbench to both provide inputs to a system under design and check outputs from the system. The testbench is typically written at the behavioral level, without any need for it to be synthesizeable, yet it is an integral part of the simulation execution.

We next consider the realism of the benchmark circuits. Figure 2 illustrates an abstract design flow for digital systems. Specific tool names have been intentionally omitted in an attempt to illustrate this as a generic flow, not any specific flow. The user input of a VHDL description is at the top. This could either be via original entry of the VHDL text or the use of a higher-level tool such as Renior™. The user level system description is simulated (e.g., using Model*Sim*®) in the right-hand path until the user is satisfied with the design at that level of abstraction. The VHDL code is then used as input to the synthesis tools (e.g., Leonardo Spectrum™), yielding a description of the system at the gate level. After place-and-route (using vendor tools), the gate level description has backannotated timing information as well. Often this gate level description is simulated (the left-hand path in the flow diagram) until the user is satisfied that it is ready for fabrication (the center path in the diagram).

Note that there are two different VHDL descriptions of the system in the figure, the first at the user level and the second at the gate level. In a more complete flow diagram, additional system descriptions might exist. It is important that the benchmark set contain circuit descriptions at a number of different abstraction levels. At a minimum, the set must contain circuits described at the user level (i.e., synthesizeable VHDL descriptions) and at the gate level (e.g., both with and without detailed timing information).

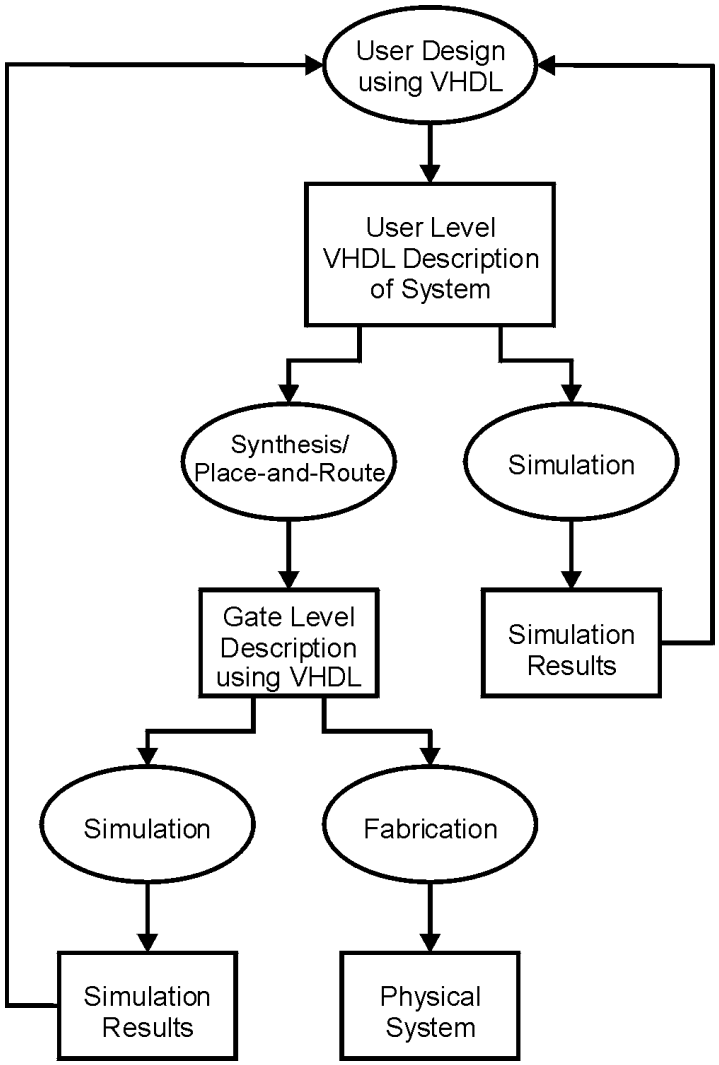

Figure 2. Generic design flow.

Finally, for the benchmark set to be effective the circuits that comprise the set must come from a variety of sources. The initial entries (described below) are all from our institution. One of the motivations of this paper is to issue an appeal to individuals that have candidate circuits to make those circuits available for inclusion in the benchmark set.

4. The SIMBENCH Logic Simulation Benchmark Set

The original entry in the SIMBENCH logic simulation benchmark set is a small processor design. The processor is the end result of the capstone design course in the undergraduate computer engineering program at Washington University [6]. This design is available both at the user level (the original VHDL description designed by the students) and at the gate level (targeted to a Xilinx XC4000 series FPGA). The user level VHDL code is comprised of 18 entity instantiations to describe the processor itself and 4 entity instantiations in the testbench used to exercise the processor. At the gate level, the processor consists of 218 CLBs on the FPGA with a total of 98 flip-flops. The testbench provides external memory, an I/O path, and an instruction

stream designed to exercise the full instruction set of the processor. A 12 million clock cycle test executes for approximately 50 minutes on a Sun UltraSparc 10 platform. The same testbench is used to exercise both the user level description as well as the gate level model.

The next three entries in the benchmark set are considerably larger in size. They are the three ASICs that form the basis of the Washington University Gigabit Switch (WUGS) [7]. The WUGS is an ATM switching system that is an open design, and is comprised of a switch element chip, an input port processor chip, and an output port processor chip.

While the above entries comprise an effective beginning, they are clearly insufficient to constitute a complete benchmark set. It is imperative that a larger collection of circuits be included if the benchmark is to be truly effective. Interested readers that have candidate designs that they would like to be included in the benchmark set are encouraged to contact the authors.

5. Conclusions

This paper describes the motivations for, features of, and current state of the SIMBENCH logic simulation benchmark set. At present, it is just getting off the ground, and additional contributions are required to make it a viable tool for the research community. The current edition of SIMBENCH can be accessed via the web at http://ccrc.wustl.edu/~simbench. With the availability of a freely distributed VHDL simulation system from the University of Cincinnati and a credible benchmark set in SIMBENCH, it is hoped that future research results in the field of parallel logic simulation will have significant relevance to commercial practice, improving the performance of simulation tools and improving the efficiency of the system design process.

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