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Performance Evaluation of a Reconfigurable, Embedded Photonic Multiring Interconnection Network*

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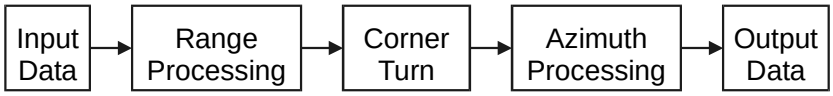
Abstract

The ever increasing demand for interconnect bandwidth in embedded parallel processors has motivated the development of photonic communications technologies that effectively support short-distance links. Electrooptical I/O to and from VLSI chips is one such photonic technology. A multiring architecture that exploits optical I/O on and off chip is described in [1]. At the heart of the system is a VLSI photonic device based on the use of an $M \times M$ array of Vertical Cavity Surface Emitting Laser (VCSEL) and detector pairs [2]. Each VCSEL-detector pair is capable of operating at rates exceeding 1 Gb/s. With $M = 32$, the raw bandwidth deliverable is greater than 1 Tb/s.

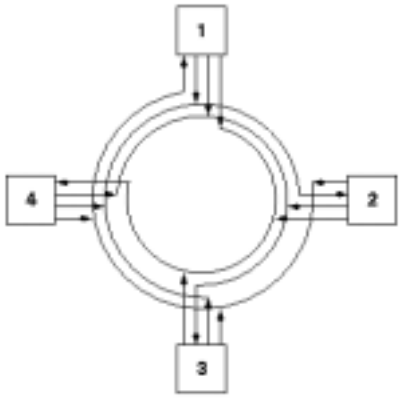
In this paper we are interested in investigating the performance gains achievable on a class of embedded signal processing algorithms through the use of reconfiguration in the processor interconnection network. The application class is the set of pipelined problems in which computation and communication occurs on a cyclic basis. An example, synthetic aperture radar (SAR) image formulation, is shown below:



In the SAR application, the first communication phase consists of data being input from the sensor array (a broadcast). The first computation phase consists of range processing. The second communication phase is a corner turn operation (an all-to-all pattern). The second computation phase is azimuth processing, and the final communication phase is the output of formulated SAR images (a reduction).

RECONFIGURABLE MULTIRING ARCHITECTURE

The multiprocessor interconnect described in [1] utilizes a multiring topology. Consider the four-node example where each processing node is connected to the multiring as illustrated below. Given the numerous VCSEL-detector pairs, we can assign disjoint subset of VCSEL-detector pairs to each processing node. If these subsets are allocated according to receiver designation, then each subset can be thought of as a channel associated with messages being received by a given node. By changing the number of VCSEL-detector pairs associated with each receiver, we can alter the bandwidth associated with that subring.



Within a subring, media access is arbitrated using the Deficit Round Robin (DRR) fairness protocol [3], which supports the assignment of arbitrary bandwidth ratios to various sources on a subring. With the ability to set receiver bandwidth via the allocation of VCSEL-detector pairs and the ability to set source bandwidth via the DRR media access protocol, the interconnect may be configured for arbitrary capacity (constrained by the total bandwidth available) for any potential flow (i.e., source-destination pair).

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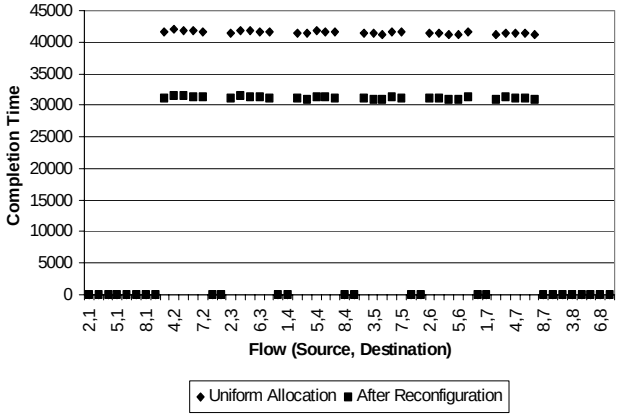
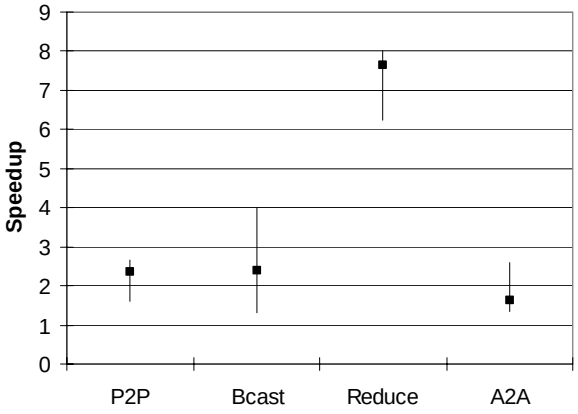
APPLICATIONS

The applications of interest are ones in which computation and communication alternate with one another. The performance results presented here are derived from 2 real applications (SAR image formation and a beam forming application) and 5 synthetic applications. The SAR image formation application is described above. The beam forming application includes the 3 communication phases in the SAR image formation and adds two additional communication phases, a reduction and broadcast. The synthetic applications have from 3 to 6 communications phases. Their communications patterns are randomly chosen from the following set: broadcast, reduce, all-to-all, and point-to-point. The flows and message sizes are also randomly generated.

PERFORMANCE RESULTS

A discrete-event simulation model was used to evaluate the performance of the reconfigurable photonic multiring. An 8 node system was simulated, with communication traffic generated according to the 2 real applications and 5 synthetic applications described above. For each application, the system was simulated twice. The initial simulation utilized a uniform bandwidth allocation to each potential flow (all source-destination pairs are allocated an equal fraction of the total bandwidth). In the second simulation the interconnection network was reconfigured at the start of each communication phase to provide an optical bandwidth allocation best suited to the communication pattern required by the algorithm in that phase. The figure on the left below shows the completion time (in simulated time units) for the second communication phase of the SAR image formulation application for both the uniform allocation and the allocation present after reconfiguration. For the corner turn, a 25% performance gain can be directly attributable to reconfiguration.





The figure on the right above shows the mean, minimum, and maximum speedup obtained for each type of communication pattern, independent of the application in which it is found. The speedup is defined as the ratio of the communication completion time with a uniform bandwidth allocation to the completion time with a reconfigured allocation. The performance improvement is significant across the board, indicating a clear benefit to reconfigurability in the interconnection network.

[1] R. Chamberlain, M. Franklin, and A. Mahajan, "VLSI Photonic Ring Interconnect for Embedded Multicomputers: Architecture and Performance," to appear in *Proc. of 14th Conf. on Parallel and Distributed Computing Systems*, August 2001.

[2] D. Plant et al., "A 256 channel bi-directional optical interconnect using VCSELs and photodiodes on CMOS," in *Proc. of Optics in Computing*, June 2000.

[3] A. Mahajan, M. Franklin, and R. Chamberlain, "Fairness Issues in an Embedded Photonic Ring Interconnect," in *High Performance Embedded Computing Workshop*, September 2000.